In the Claims:

1. (Previously Presented) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a bit line on the first interlayer dielectric that is electrically connected to the transistor;

a capacitor electrically connected to the plug, the capacitor having a first bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode; and

a reaction buffer layer between the first interlayer dielectric and the capacitor-ferroelectric layer;

wherein at least one of the capacitor or the reaction buffer layer is on the bit line.

2. (Previously Presented) The ferroelectric memory device of Claim 1, wherein the reaction buffer layer is adjacent to the side surfaces of the first bottom electrode, and wherein a top surface of the reaction buffer layer and the top surface of the first bottom electrode form a planar surface.

3. (Previously Presented) The ferroelectric memory device of Claim 2, further comprising a third interlayer dielectric under the reaction buffer layer and on at least one of the side surfaces of the first bottom electrode, and wherein the reaction buffer layer comprises a material that prevents a reaction between the third interlayer dielectric and the capacitor-ferroelectric layer.

4. (Original) The ferroelectric memory device of Claim 2, wherein the reaction buffer layer is formed of a material selected from the group consisting of titanium oxide, tantalum oxide and aluminum oxide.

5. (Previously Presented) The ferroelectric memory device of Claim 3, wherein the a third interlayer dielectric is recessed between the first bottom electrode and a second bottom electrode associated with a capacitor of an adjacent ferroelectric memory device.

6. (Previously Presented) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a capacitor electrically connected to the plug, the capacitor having a first bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode;

a reaction buffer layer between the first interlayer dielectric and the capacitor-ferroelectric layer;

a bit line that is electrically connected to the transistor on the first interlayer dielectric; and

a third interlayer dielectric recessed between the first bottom electrode and a second bottom electrode associated with a capacitor of an adjacent ferroelectric memory device;

wherein the reaction buffer layer is adjacent to the side surfaces of the first bottom electrode, wherein a top surface of the reaction buffer layer and the top surface of the first bottom electrode form a planar surface and wherein the reaction buffer layer is on the third interlayer dielectric.

7. (Previously Presented) The ferroelectric memory device of Claim 6, further comprising a second interlayer dielectric between the first interlayer dielectric and the third interlayer dielectric, wherein the plug further penetrates the second interlayer dielectric to electrically connect the first bottom electrode to the semiconductor substrate.

8. (Previously Presented) The ferroelectric memory device of Claim 1, further comprising a first diffusion barrier between the first interlayer dielectric and the reaction buffer layer and on at least one of the side surfaces of the first bottom electrode.

9. (Original) The ferroelectric memory device of Claim 8, wherein the first diffusion barrier comprises an oxygen diffusion barrier.

10. (Previously Presented) The ferroelectric memory device of Claim 1, wherein the first bottom electrode comprises:

a first material that serves as an oxygen diffusion barrier;

a second material for providing the capacitor-ferroelectric layer with oxygen on the first material; and

a third material having a lattice point that allows for formation of a capacitor-ferroelectric layer having a crystalline structure.

11. (Original) The ferroelectric memory device of Claim 10, wherein the first material is iridium, the second material is iridium oxide, and the third material is platinum.

12. (Original) The ferroelectric memory device of Claim 1, wherein the top electrode comprises a fourth material for providing the capacitor-ferroelectric layer with oxygen and a fifth material that is selected to improve the strength of the fourth material.

13. (Original) The ferroelectric memory device of Claim 12, wherein the fourth material is on the capacitor-ferroelectric and the fifth material is on the fourth material.

14. (Original) The ferroelectric memory device of Claim 12, wherein the fourth material is iridium oxide, and the fifth material is iridium.

15. (Original) The ferroelectric memory device of Claim 12, further comprising a second diffusion barrier on the capacitor-ferroelectric layer and on the top electrode.

16. (Original) The ferroelectric memory device of Claim 15, wherein the second diffusion barrier acts as a hydrogen diffusion barrier.

17. (Original) The ferroelectric memory device of Claim 16, wherein the second diffusion barrier comprises an aluminum oxide layer.

18. (Previously Presented) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a capacitor electrically connected to the plug, the capacitor having a bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode;

a reaction buffer layer between the first interlayer dielectric and the capacitor-ferroelectric layer;

a fourth interlayer dielectric on the top electrode;

a first metal line on a part of the fourth interlayer dielectric;

a fifth interlayer dielectric on the fourth interlayer dielectric;

a via hole that exposes the top surface of the top electrode; and

a second metal line in the via hole that is electrically connected to the top electrode.

19. (Original) The ferroelectric memory device of Claim 18, wherein the first metal line and the second metal line each comprise an aluminum metal line.

20. (Original) The ferroelectric memory device of Claim 5, further comprising a first contact pad between the bit line and the semiconductor substrate.

21. (Original) The ferroelectric memory device of Claim 20, wherein the first contact pad comprises a polysilicon contact pad.

22. (Original) The ferroelectric device of Claim 21, further comprising a second contact pad between the plug and the semiconductor substrate.

23-48. (Cancelled).

49. (Currently Amended) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a capacitor electrically connected to the plug, the capacitor having a bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode; ~~and~~

a third interlayer dielectric layer on the first interlayer dielectric and on at least one of the side surfaces of the bottom electrode; and

a reaction buffer layer between the third interlayer dielectric and the capacitor-ferroelectric layer;

wherein a top surface of the third interlayer dielectric is lower than the top surface of the bottom electrode.

50. (Cancelled)

51. (Previously Presented) The ferroelectric memory device of Claim 49, wherein the capacitor ferroelectric layer comprises a continuous layer that acts as a dielectric layer for at least the capacitor and a second capacitor.

52. (Currently Amended) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a capacitor electrically connected to the plug, the capacitor having a bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode;

a third interlayer dielectric layer on the first interlayer dielectric and on at least one of the side surfaces of the bottom electrode;

a reaction buffer layer between the third interlayer dielectric and the capacitor-ferroelectric layer; and

~~The ferroelectric memory device of Claim 49, further comprising~~ a bit line that is

electrically connected to the transistor, wherein at least one of the capacitor or the reaction buffer layer is on the bit line.